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Study of Logic Gates Using Quantum Cellular Automata

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Abstract - The power consumption of MOS technology device can be reduced by scaling the devices. The technology also tries to improve speed by working on the already existing technology. The need for new technology is fast approaching as Moore's law cannot hold good for next few years. For the same purpose we should turn to quantum logic and quantum cells. Quantum cellular automaton is one such technology. Though the technology is in its primitive stage, many people are working in this field. After a breakthrough in the physical implementation of the basic quantum cell the new technology is mainly focused on implementing digital designs. This article is trying to review and implement the basic gates in quantum cellular automata. Implementation is done in QCA Designer provided by University of British Columbia.

Index Terms - Quantum cells, Quantum dots , Offset

I. Introduction

In VLSI fabrication, the chip size has been reduced dramatically but it cannot be reduced further, as this will lead to more power consumption by means of sub threshold leakage current. The new technology QCA is considered as an option for reducing power consumption. Quantum cellular automata have been an area of research for a long time. But it gained focus only after a physical implementation of the same recently. The field is starting to get attention recently also because it is more focused on to VLSI technology. The conventional MOS technology is supposed to be completely replaced with quantum cellular automata in coming decades.

Devices based on quantum mechanism is more fast and power efficient as it works in smallest physical form that is atomic level and only uses current in the range of nano amperes. Quantum cells are based on superposition and entanglement principle. The basic necessity of achieving low power consumption which the researchers in the field of VLSI are trying to accomplish with QCA technology. The Quantum cells based research is carried out in very broad area such as testing [3][16], reversible logic implementation in QCA [5], majority gate design[7],[9], complex combinational circuit design [8], AND OR Invert logic design [10], binary wire is illustrated in [12], description of QCA tool is given in [13], quantum computation is explained in[14], application of QCA in microelectronics is illustrated in [15]. This paper will be explaining the basic QCA cell and will be reviewing basic gates with QCA model. The article reviews universal gates in terms of QCA layout. The same gates are implemented and simulation results are produced.

II. Quantum Cell

A. Cell

The basic quantum cell consist of 5 quantum dots placed on a square, four on the corners and one in the center [1][14].There are two electrons which are free to move across the quantum dots. For stability the electrons always occupy the diagonally opposite dots (antipodal outer sites). The potential barrier across the cell is assumed to be large enough to block the intercellular tunneling [11]. The schematic of the basic five site cell is shown in Fig.1. and the logic states represented by electronic position is shown in Fig.2.

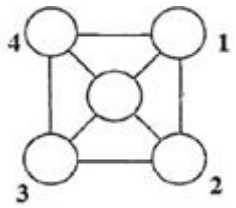

Fig. 1. Schematics of a basic five- site cell with 'X' orientations

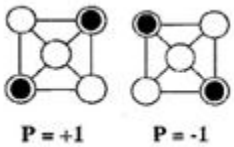

Fig. 2. Electrons occupying antipodal sites in a cell, this type of orientation is the most stable form. This bistable states is denoted by '+1' and '-1' [1][4][6].

III. Universal Logic Gates

A. NAND Logic Gate

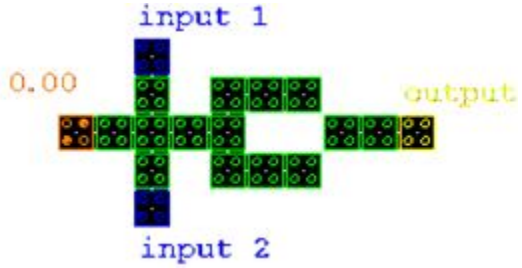

Fig. 3. The NAND gate is implemented without offset by combining a programmable gate and an inverter

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NAND gate is implemented by placing an inverter at the output of the AND gate this can be done by two methods by simply giving the output cell an offset equal to half the cell width (which is 10nm in the current experiment) or implementing a inverter with no offset between the input and output . The fixed state of programmable gate is '0'. The layout of NAND gate without offset is shown in Fig.3. and with offset is shown in Fig.4.

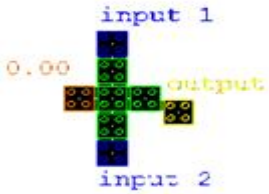

Fig. 4. NAND gate implementation - Offset cell at the output inverts the signal from reduced programmable cell

B. NOR Logic Gate

NOR gate implementation is similar to NAND gate, the fixed state for the reduced programmable gate is set to '1' instead of '0' set for the NAND gate. NOR gate can also be implemented by two types of arrangements either by combination of programmable gate and an inverter or by arranging the output cell with an offset [2]. The output for implementation without offset is at a range of 9ev.
The layout of NOR gate without offset is shown in Fig.5 and with offset is shown in Fig.6.

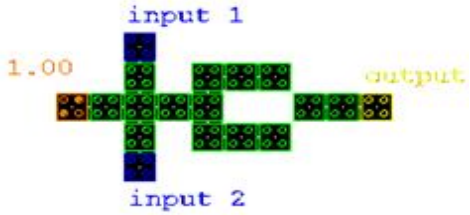

Fig. 5. The arrangement is combination of inverter and a programmable gate without offset.

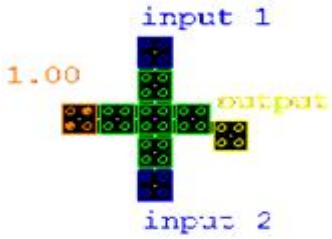

Fig. 6. NOR gate can be also implemented by offset arrangement where the output cell is aligned partially with the programmable gate, which inverts the signal and we get inverted combined with an OR gate which produces a NOR logic [2].

IV. Results And Discussions

With QCADesigner ver.2.0.3, the logical structure functionality is verified. Bistable approximation is done where Cell size is 20nm, Scale factor for all cells is '1', Clock high is 9.8e-22J, Clock low is 3.8e-23J,Upper Threshold of 0.5000, 12000 number of samples, Lower Threshold of -0.5000. The simulation results obtained using QCA Designer is shown in Fig.7-10 for universal gate logics that are discussed above.

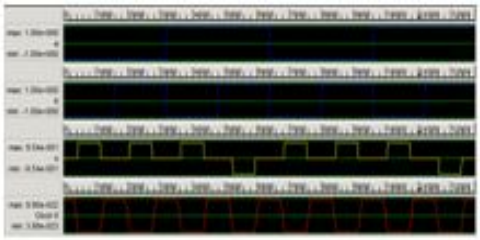

Fig. 7. The output for NAND gate without offset of the cells

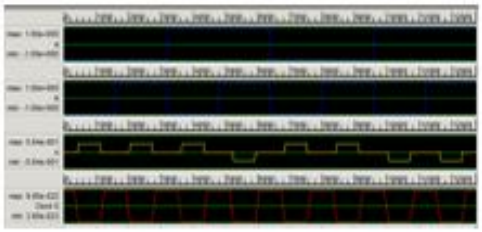

Fig. 8. The output for NAND gate with offset output cell.

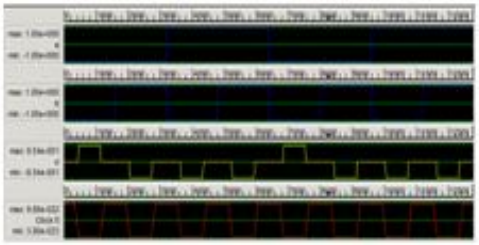

Fig. 9. The output for NOR gate without offset cell as output

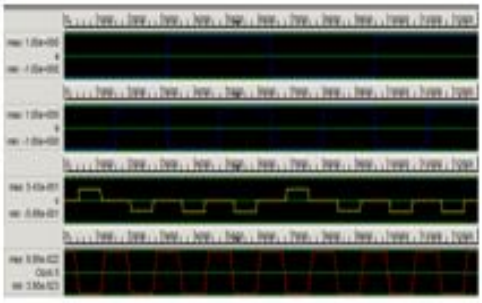

Fig. 10. The output for NOR gate with offset cell at the output side.

Offset in the explanation reference to 10nm shift in cell compared to the cells coming from the input for all cases unless specified. The output value for NAND and NOR gates with and without offset structures are compared in Table I and Table II respectively.

Table I. The Output Value For NAND Gate With Offset Is Compared To Without Offset Layout

Gate structure	Output (max, min)
Without offset	9.54e,-9.54e
With offset	5.64e,-5.64e

Table II. The Output Value For NOR Gate With Offset Is Compared To Without Offset Layout

Gate structure	Output (max, min)
Without offset	9.54e,-9.54e
With offset	5.43e,-5.68e

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The layout without offset gives maximum output, where as the layout with offset gives reduced output.

Conclusion

Logic gates can be easily implemented with quantum cellular automata. The system will get drastically reduced in size and hence power consumption will decrease as per principle of low power VLSI design. The offset placement of cell gives a reduced output signal but signal is more precise and fine edged for layout where there is no offset between the cells that is cells are organized either horizontally or vertically. Complex systems can be implemented at a very smaller size with low power consumption and more performance in Quantum Cellular Automata. The position of cells has an effect on gate output. Thus the article reviewed the universal logic gates and implemented using QCA Designer.

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